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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/965,534 | 09/25/2001 | Katsushi Nagaba | 81790.0219 | 3774 |

26021 7590 08/27/2004

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| EXAMINER | |
|---|---|
| ABRAHAM, FETSUM | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/965,534 | NAGABA ET AL. | |
| | Examiner | Art Unit | |
| | Fetsum Abraham | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## Claims rejection

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens (6,173,345).**

As for claims 1 and 5, the patent discloses an integrated circuit in figure 2 composed of register circuits receiving data and outputting data based on control clock signals having, a delay register circuit (249) that receives data from the serial controller (248) and ID register (247) and outputs delay adjusted data of the data inputs, a variable delay circuit block ((244) that received the delayed outputs that further adjusts the delayed signals by introducing delay, and a driver circuit (242) that drives another stage of the overall circuit after receiving the delay signals from the variable delay circuit through the multiplexer (245).

Although the prior art may have omits to fully describe what might dictate the terms of data patterns in such circuit configurations, it would have been obvious to one skilled in the art to expect the delayed signals heavily depending on the input data patterns, since input data patterns such as data frequencies (variable in nature) dictate the terms of output data patterns.

As for claims 2,6, the incoming data signals into variable delay circuit are read data signals in that specific relationship and the driver circuit accepting data from the

variable delay circuit is a peripheral element out of the variable delay circuit. It is also clear that driver circuits that receive signals from other circuits could either be internal or external depending on application.

As for claim 3, write and read functions are inherent to memory structures such as the circuit in the patent. Buffer circuits normally facilitate data write/read functions. Clearly, the memory structure is capable of writing any signal at the output of the driver.

As for claim 4, part of the delayed data in the structure is address signals coming from ID driver block (247) and fed into the delay circuit (249).

As for claim 7, so long as said first and second data, delay circuits and driver circuits are not integrated to produce a composite result based on the interdependence of both data signals, they are considered multiple circuits of the same function in integration. In this case, the circuitry and function of a single integrated circuit can be duplicated in multiple independent configurations in the same base substrate in order to avoid circuit density and save substrate material.

As for claims 8-10, the issue again boils down to multiplicity, which is common in the art particularly in memory arrays like in the prior art. The outstanding issues of writing and reading data have already been discussed in single circuit configuration environment.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham
11/26/03